CLAIMS:

1. A method of manufacturing a semiconductor device having an insulated gate type field effect transistor, comprising the steps of:

forming a gate insulating film and an electrode layer on a semiconductor substrate;

patterning said electrode layer to form a gate electrode layer having a predetermined area and facing said semiconductor substrate with said gate insulating film being interposed therebetween;

forming an interlayer insulating film covering said gate electrode layer;

forming a wiring layer connected to said gate electrode layer on said interlayer insulating film;

forming a conductive material layer on said wiring layer;

coating a resist layer on said conductive material layer;

patterning said resist layer to form a resist mask forming a wiring pattern having an antenna ratio of about ten times or more relative to said predetermined area of said gate electrode layer facing said semiconductor substrate;

first plasma-etching at least said conductive material layer by using said resist mask as an etching mask;

removing said resist mask after said first plasma-

etching step; and

after removing said resist mask, second plasma-etching at least part of said wiring layer connected to said gate electrode layer.

2. A method according to claim 1, wherein said interlayer insulating film includes a plurality of insulating films interposing another wiring layer therebetween.

3. A method according to claim 1, wherein said conductive material layer is made of carbon.

4. A method according to claim 3, wherein said removal step is performed by oxygen plasma down-flow.

5. A method according to claim 1, wherein said first plasma-etching step etches said conductive material layer, and said second plasma-etching step etches said wiring layer by using said conductive material layer as an etching mask.

6. A method according to claim 1, wherein said first plasma-etching step etches said conductive material layer and the main part of said wiring layer, and said second plasma-etching step etches the remaining part of said wiring layer.

7. A method of manufacturing a semiconductor device

having a conductive film pattern with a pattern space of 1 μm or less, comprising the steps of:

forming an electrode layer on part of the surface of a semiconductor substrate, with a thin insulating film being interposed therebetween;

forming an interlayer insulating film on said electrode layer;

forming a conductive film connected to said electrode layer on said interlayer insulating film;

forming an insulating material mask layer on said conductive film;

coating a resist layer on said insulating material mask layer;

patterning said resist layer;

patterning said insulating material mask layer by using said resist layer as an etching mask;

removing said resist layer; and

plasma-etching and patterning said conductive layer by using said insulating material mask layer as an etching mask, wherein the thickness of said insulating material mask layer is set to a half or less of a minimum pattern space.

8. A method according to claim 7, wherein said interlayer insulating film has a contact hole exposing said electrode layer.

9. A method according to claim 7, wherein said interlayer insulating film includes a plurality of insulating films interposing another wiring layer therebetween.

10. A method of manufacturing a semiconductor device, wherein in etching a wiring layer connected to an insulated gate of an insulated gate type field effect transistor or an insulating layer on the wiring layer by using plasma having uniform characteristics and exposed on the surface of a material to be processed, an RF bias having a frequency of 1 MHz or lower is applied to said material to be etched so as to make the amounts of ions and electrons incident in generally the vertical direction upon the surface of said wiring layer, generally equal to each other.

11. A method according to claim 10, wherein a divergent magnetic field gradually reducing magnetic flux densities and a mirror field are applied to said material to be processed.

12. A method of manufacturing a semiconductor device, wherein plasma is generated under a divergent magnetic field gradually reducing a magnetic flux density and exposed on the surface of a material to be processed, and a cusp magnetic field is applied so as to make the amounts of ions and electrons incident generally in the vertical direction upon the surface of

said material to be processed, generally equal to each other.

13. A method of manufacturing a semiconductor device for forming a first wiring layer and a second wiring layer at the same time, said first wiring layer being connected to a gate electrode on a gate insulating film formed on a semiconductor region, and said second wiring layer being connected to said semiconductor region, wherein in patterning said first and second wiring layers, a third wiring layer electrically separated from and placed between said first and second wiring layers is left unetched.

14. A method according to claim 13, wherein the spaces among said third, first, and second wiring layers are set generally equal to a minimum pattern space of said third, first, and second wiring layers.

15. A semiconductor device comprising:

a semiconductor substrate;

an insulated gate structure formed on said semiconductor substrate;

an interlayer insulating film covering said insulated gate structure;

a first wiring and a second wiring formed on said interlayer insulating film, said first wiring being connected to said gate structure, and said second wiring being disposed

spaced apart from said first wiring; and

a wiring layer including an interpolation-wiring region not used as a wiring, said wiring layer being formed between said first and second wirings with generally the same spaces being set between said first and second wirings and said wiring layer.